

What is claimed is:

1 1. A method for generating a refresh clock of a DRAM
2 module, wherein the DRAM module comprises a plurality of memory
3 cells, each of the memory cells having a storage capacitor,
4 comprising:

5 providing a dummy capacitor, the dummy capacitor has a
6 positive correlation with the storage capacitor;
7 and

8 generating a refresh clock according to a capacitance
9 of the dummy capacitor;

10 wherein a refresh interval of the refresh clock is
11 positively correlated with the capacitance of the
12 dummy capacitor.

1 2. The method for generating a refresh clock of claim
2 1, further comprising a method for generating the refresh clock:
3 providing an oscillator for generating the refresh clock,
4 wherein the dummy capacitor is an oscillator load.

1 3. The method for generating a refresh clock of claim
2 1, wherein the dummy capacitor is one of the storage capacitors.

1 4. A refresh clock generator of a DRAM module, wherein
2 the DRAM module comprises a plurality of memory cells, each
3 of the memory cells having a storage capacitor, comprising:
4 a dummy capacitor positively correlated with the storage
5 capacitor; and
6 a clock generator for generating a refresh clock, and
7 coupling to the dummy capacitor;

8 wherein a refresh interval of the refresh clock is
9 positively correlated with a capacitance of the
10 dummy capacitor.

1 5. The refresh clock generator of claim 4, wherein the
2 clock generator is a ring oscillator and the dummy capacitor
3 is a ring oscillator load.

1 6. The refresh clock generator of claim 5, wherein the
2 refresh clock generator comprises a plurality of dummy
3 capacitors, the ring oscillator comprises a plurality of
4 inverters, and each output terminal of the inverters couples
5 to a corresponding dummy capacitor.

1 7. The refresh clock generator of claim 4, wherein the
2 dummy capacitor is one of the storage capacitors.